

# Examination WS 17/18

## Communication Systems and Protocols



Institute for Information Processing Technologies - ITIV  
Prof. Dr.-Ing. Dr. h. c. Jürgen Becker

### Communication Systems and Protocols

Date: 13.02.2018  
Name: Test Name  
Matr. ID: 1234567  
ID: 1

Lecture Hall: ITIV  
Seat: 1

## Prerequisites for the examination

### Aids:

- A single sheet of A4 paper with **self- and hand-written** notes. Writing may be on both sides
- A dictionary
- A non-programmable calculator.
- Writing utensils
- Use only indelible ink - use of pencils and red ink is prohibited.
- Other material than that mentioned above, is strictly forbidden. This includes any type of communication to other people.

### Duration of the examination:

The exam duration is 120 minutes.

### Examination documents:

The examination comprises 30 pages (including title page, 8 blocks of tasks).

Answers may be given in English or German. A mix of language within a single (sub)-task is not allowed.

**Please check your matriculation number and id on every page before processing the tasks.**

In your solution mark clearly which part of the task you are solving. Do not write on the backside of the solution sheets. If additional paper is needed ask the examination supervisor.

### End of Exam:

You will not be allowed to hand in your examination and leave the lecture hall in the last 30 minutes of the examination. At the end of the examination: Stay at your seat and put all sheets (including this title page) into the envelope. Only sheets in the envelope will be corrected. We will collect the examination.

	Page	≈ Pts. [%]	Points
Task 1: Physical Basics	2	12	<b>15</b>
Task 2: Transmission Principles	6	12	<b>15</b>
Task 3: Modulation and Spread Spectrum	10	11	<b>13</b>
Task 4: Media Access	15	12	<b>14</b>
Task 5: Error Protection	18	12	<b>15</b>
Task 6: Protocols	21	12	<b>14</b>
Task 7: Routing	25	12	<b>14</b>
Task 8: Network Topologies	28	13	<b>16</b>
			Σ <b>116</b>

# Task 1: Physical Basics

## Task 1.1: Drivers

- A) Insert the logic level (H/HIGH, L/LOW, Z/HIGH-IMPEDANCE) of the output and the state of the transistors (C/conducts, B/blocks) into the table according to the input configuration  $x_1$  and  $en$  at the tri-state TTL output driver.

2

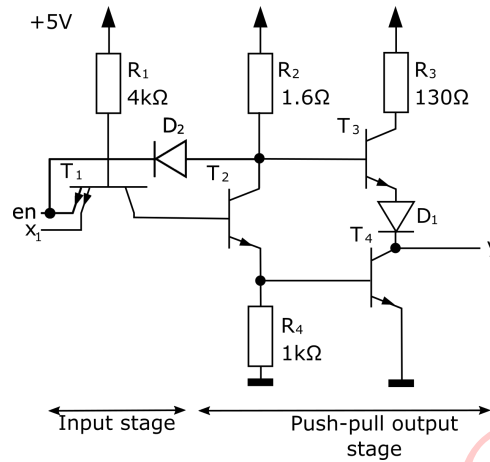


Figure 1.1: Tri-state TTL output driver

$x_1$	$en$	$T_1$	$T_2$	$T_3$	$T_4$	$y$
L	L	conducts	blocks	blocks	blocks	Z
H	L	conducts	blocks	blocks	blocks	Z
L	H	conducts	blocks	conducts	blocks	H
H	H	blocks	conducts	blocks	conducts	L

-0.5pt per wrong cell,  
consider consequential  
errors

- B) List two advantages of using TTL drivers over open-collector drivers.

1

High currents are possible / low output resistance when driving high  $\rightarrow$  fast switching; 0.5pt per advantage

No/little energy is consumed while static (esp. while driving low)

## Task 1.2: AD Conversion

One way of implementing the AD-conversion is the flash converter. A 2-bit flash converter is shown in Figure 1.2.

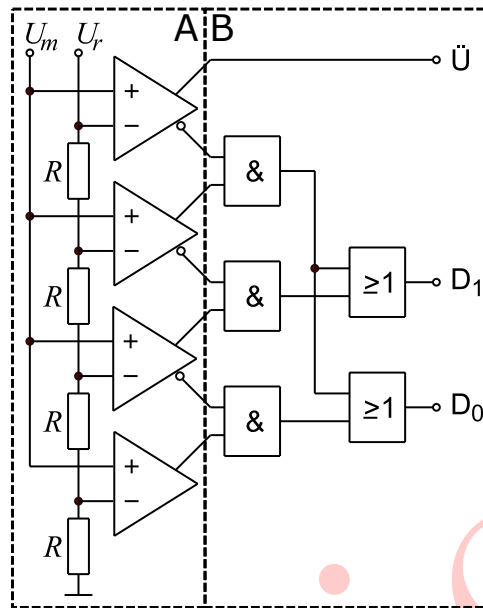


Figure 1.2: Flash Converter

- A) Briefly explain the the working principle of a flash converter. What happens in sections A and B? What is the purpose of the resistor cascade?

3

- A** Input voltage is compared to multiple reference voltages in parallel. The reference voltages are generated using the resistor cascade. +1pt for function of resistor cascade  
+1pt for comparison to multiple reference
- B** Binary encoder, which generates the binary value based on the comparator output. voltages in parallel  
+1pt for binary value calculation

B) Name one advantage and one disadvantage of the flash converter.

1

- + very fast / high sampling rate
- + simple structure
- + simple concerning timing requirements
- high cost with increasing precision
- high energy consumption with increasing precision
- many comparators needed with increasing precision

-0.5pt per  
wrong/missing  
(dis)advantage

### Task 1.3: Reflections on wires

In figure 1.3 a transmission system is given. It consists of a voltage source of unknown voltage  $U_q$  (including an internal resistance  $R_i$ ), a signal line of length  $L$  and a resistor  $R_L$  as receiver. The signal propagates with speed  $v$ .

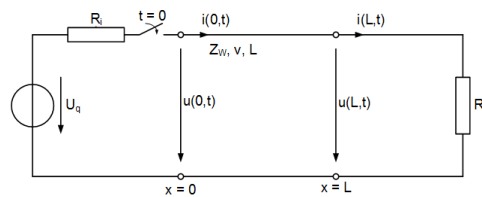


Figure 1.3: Transmission system

For varying  $R_i$  and  $R_L$  the following signal diagrams (figure 1.4) can be drawn. They are showing the voltage  $u(0,t)$  at the beginning of the signal line and the voltage  $u(L,t)$  that can be measured at the end of the line.

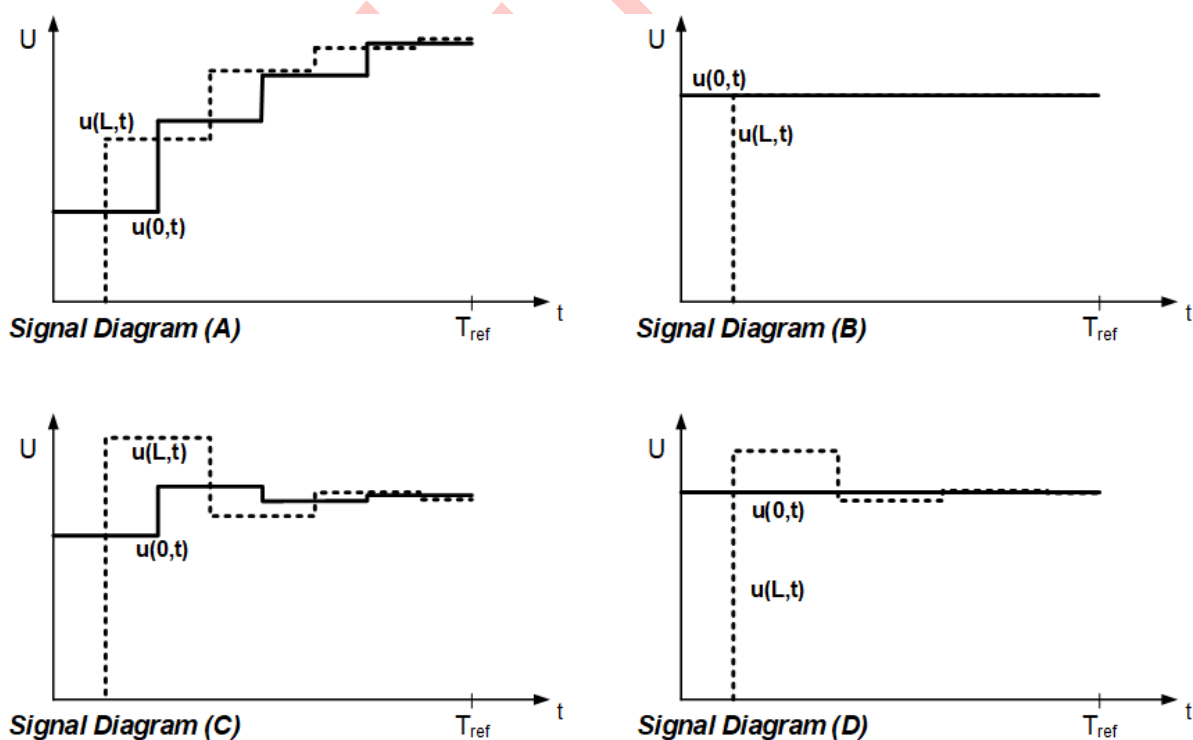


Figure 1.4: Voltages on signal line

- A) In which of the examples given in figure 1.4, if any, is the line terminated correctly with a suitable value of  $R_L$ ? Justify your answer.

1

In signal diagram B, because there is no reflection at the end of the wire.  $U(L, t)$  equals  $U(L, 0)$  after the first time step. **1pt for correct answer**

- B) For each of the signal diagrams denote in the following table:

4

- Is the reflection factor  $r_i$  at the beginning of the signal line negative, positive, or zero?
- Is the reflection factor  $r_L$  at the end of the signal line negative, positive, or zero?

If the reflection factor cannot be determined from the signal diagram, indicate this with a dash (–).

	$r_i$ [neg, pos, 0, –]	$r_L$ [neg, pos, 0, –]
Signal diagram (A)	pos ( $r_i = +0.2$ )	pos ( $r_L = 0.8$ )
Signal diagram (B)	–	0 ( $r_L = 0$ )
Signal diagram (C)	neg ( $r_i = -0.5$ )	pos ( $r_L = +0.6$ )
Signal diagram (D)	neg ( $r_i = -1$ )	pos ( $r_L = +0.2$ )

0.5pt per correct cell

- C) Now assume that  $R_i = 25\Omega$ ,  $R_L = 150\Omega$ , and  $Z_W = 50\Omega$ . To terminate the line properly at  $R_L$ , another resistor  $R_t$  shall be added to  $R_L$ . Does this resistor have to be added in series or in parallel to  $R_L$ ? Give a short explanation.

1

In parallel since  $R_L > R_W$  and for proper termination the combined resistance of  $R_L$  and  $R_t$  has to be equal to  $R_W$ . **1pt for correct answer**

- D) Calculate  $R_t$  such that the line is properly terminated assuming the values given above.

2

$$\begin{aligned}
 Z_W &= R_L || R_t \\
 \frac{1}{Z_W} &= \frac{1}{R_L} + \frac{1}{R_t} \\
 \frac{1}{R_t} &= \frac{1}{Z_W} - \frac{1}{R_L} \\
 R_t &= \frac{1}{\frac{1}{Z_W} - \frac{1}{R_L}} = \frac{1}{\frac{1}{50\Omega} - \frac{1}{150\Omega}} = 75\Omega
 \end{aligned}$$

**+1pt for correct formula  $\frac{1}{R_t} = \dots$   
 +0.5pt for correct formula  $R_t = \dots$   
 +0.5pt for correct numbers**

## Task 2: Transmission Principles

### Task 2.1: Line Codes

- A) We want to transmit the bit string 1010 1110 0001 through a serial wire communication channel. Complete Figure 2.1 with the digital signals transmitted using each encoding scheme.

3

0.5p for each correct  
line code

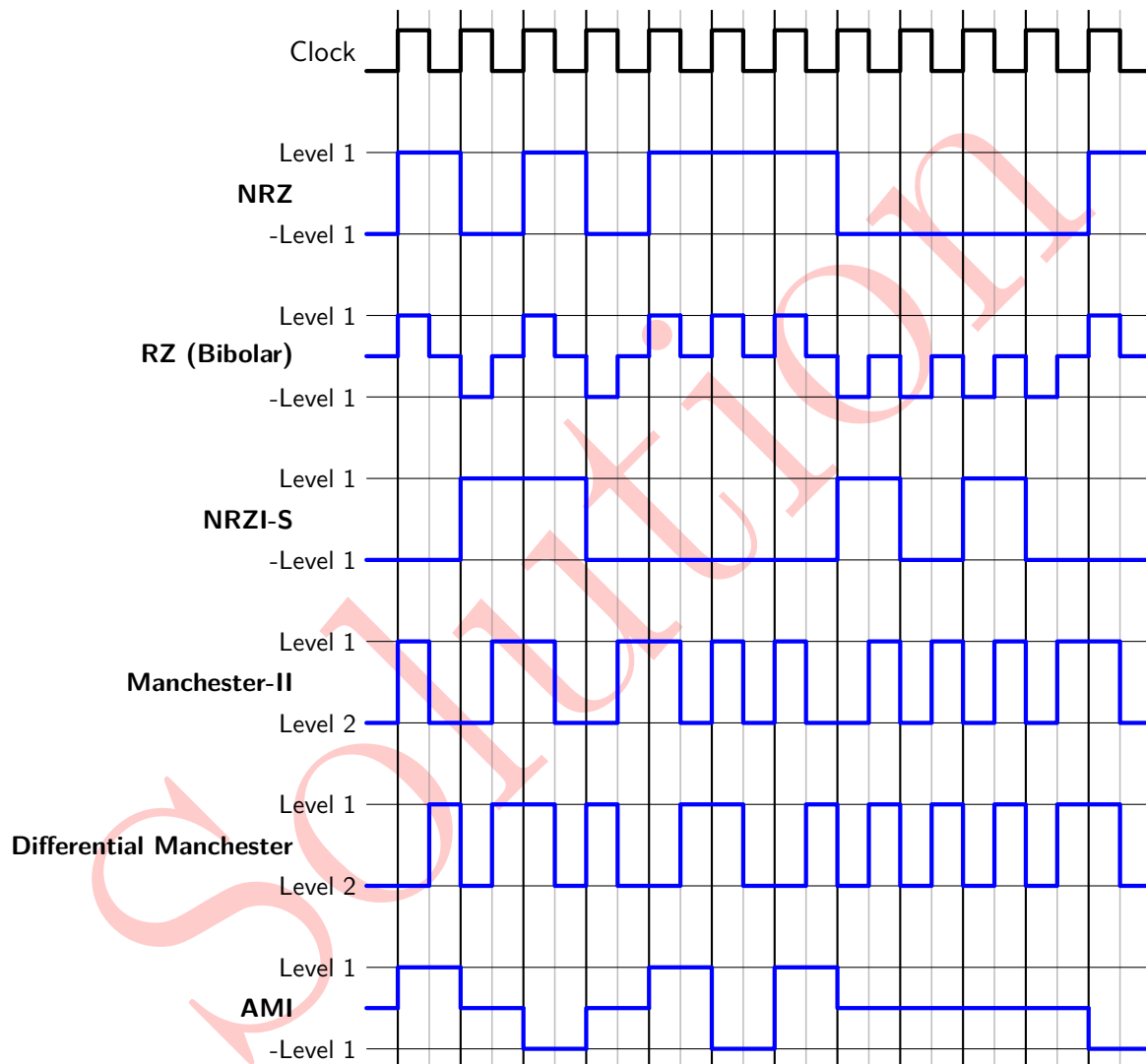


Figure 2.1: Line codes

- B) Manchester-II (Bipolar), Differential Manchester (Bipolar) and AMI are examples of codes that do not have DC components in their frequency spectrum. Explain why they present such a characteristic. Be concise.

**1**

Manchester and Differential Manchester (if Bipolar), and AMI coding do not have DC components in their frequency spectrum as each positive signal level is necessarily accompanied by a negative signal level and the average signal value is 0 over time.

**1p for showing that every positive signal accompanies a negative signal.**

- C) Among the codes in Figure 2.1, Bipolar RZ, Differential Manchester and Manchester-II require a larger Bandwidth to transmit the same message. Explain why that happens. Be concise.

**1**

Bipolar RZ, Manchester and Differential Manchester codes need a larger bandwidth for the transmitted signal as they require more transitions per bit interval.

**1p for mentioning higher number of transitions per bit**

- D) Given the transmission of a random sample signal, which codes in Figure 2.1 do not enable clock recovery of the transmitter's frequency? What is the common reason that prevents clock recovery in all codes? Be concise.

**2**

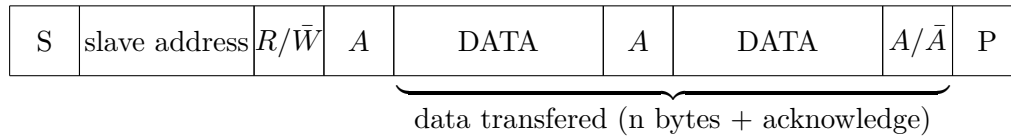
Codes: NRZ, NRZI-S, AMI.

**1p for codes.  
1p for explanation.**

For each code, there is a possible input sequence that keeps the transmission line level constant, allowing for clock skew and loss of synchronization on the receiving end.

## Task 2.2: I<sup>2</sup>C Arbitration

In this task we want to investigate the data transmission on the I<sup>2</sup>C-Bus. The simplified packet format is given in Figure 2.2. Three master nodes are simultaneously trying to transmit or read one byte of data to or from different slaves over the I<sup>2</sup>C-Bus.



term	description
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave ('0')
$\bar{A}$	not acknowledge ('1')
DATA	8-bit data
P	stop Condition

Figure 2.2: I<sup>2</sup>C-Bus frame format

A) In an I<sup>2</sup>C multimaster configuration, who is responsible for performing the arbitration?

1

The arbitration on a Multimaster I<sup>2</sup>C bus line is performed by each master.

1p for each master  
being responsible

B) What are the steps taken to perform the arbitration in an I<sup>2</sup>C multimaster interface?  
Explain briefly step by step the process by which the arbitration is performed.

1

(1) The master writes its output to the bus.

(2) The master reads back the bus line.

(3) Compares it to the output it wrote.

(4) If the line is different (wrote '1', line is '0'), then it stays passive.

1p for master reading  
back and comparing to  
value it sends

C) Consider an I<sup>2</sup>C multimaster configuration, what happens if two masters address the same slave? Explain your answer.

1



If both masters wrote the same value, no collision will be detected. In case of a "collision detection" within the data field one master recognize a different value on the SDA, because of the pull-up transistors on the line. The master with the dominant level (zero) wins the arbitration.

**1p for arbitration over data field**

Solution

- D) The addresses of the slaves, communication mode (R/ $\overline{W}$ ) and the data to be sent or read to or from them is shown in the Table 2.1. Complete the signal diagram in the Figure 2.3.

4

node	slave address	R/ $\overline{W}$	data
Master 1	0001101	1	10101100
Master 2	0101010	0	11001110
Master 3	0101011	1	01010101

Table 2.1: I<sup>2</sup>C Communication Parameters

1P for  
address+R/W+A  
1P for data+A 1P for P  
1p for correct SDA line  
consider subsequent  
failure for SDA

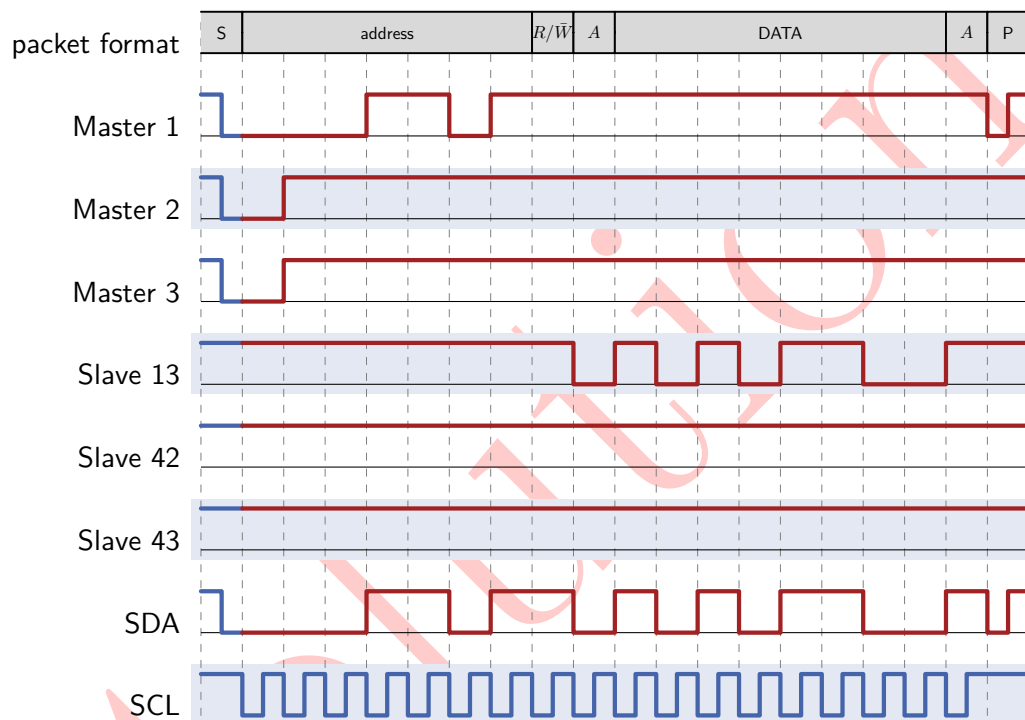


Figure 2.3: Signal sequence

- E) How many nodes can be connected to the I<sup>2</sup>C bus at maximum? Justify your answer!

1

Maximum of  $2^7 = 128$  nodes can be connected to the bus when neglecting the reserved addresses in the 7 bit address tag of the I2C frame.

+1P only with  
justification! 128-16  
reserved addresses =  
112 is also correct!

# Task 3: Modulation and Spread Spectrum

## Task 3.1: Modulation

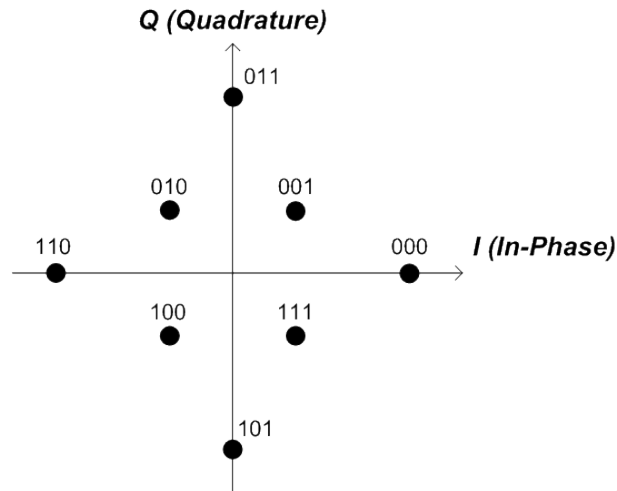


Figure 3.1: The constellation diagram of an unknown modulation

- A) The constellation diagram of an unknown modulation is shown in the Figure 3.1. Which modulation scheme is used?

1

It is the cons. diagram of 8-QAM

0.5 point for QAM-only,  
1 point for 8-QAM

- B) Assume that you have a bistream of information, i.e. **101011000111...**, which you want to modulate using 256-Quadrature Amplitude Modulation (256-QAM) technique. How many bits does the 256-Quadrature Amplitude Modulator have to read for each symbol?

1

8 (eight) bits

one point or nothing

- C) A constellation diagram of 4-QAM is shown below (Figure 3.2). You have information bits **1100110** which will be encoded starting from the left to the right. The Figure 3.3 shows the in-phase carrier signal (B), in-phase symbol (A), and in-phase modulated signal (C). Moreover, the Figure 3.4 shows the quadrature carrier signal (E), quadrature symbol (D), quadrature modulated signal (F). Use the Figure 3.3 (A and C) and Figure 3.4 (D and F) to sketch the waveforms of symbol representations and modulated information signals seen from in-phase and quadrature axes. The symbol period is twice as long as the period of carrier signal.

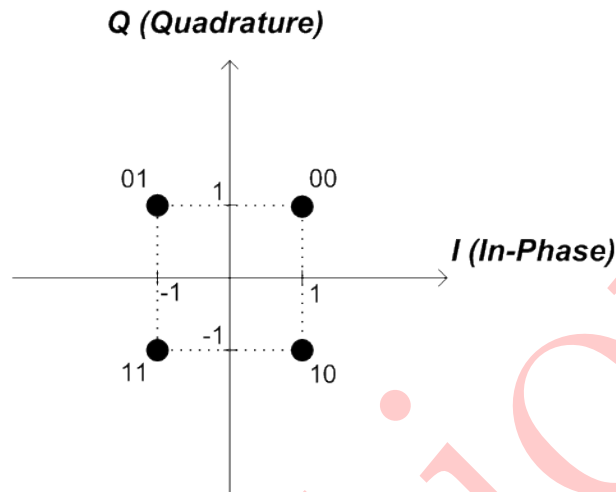
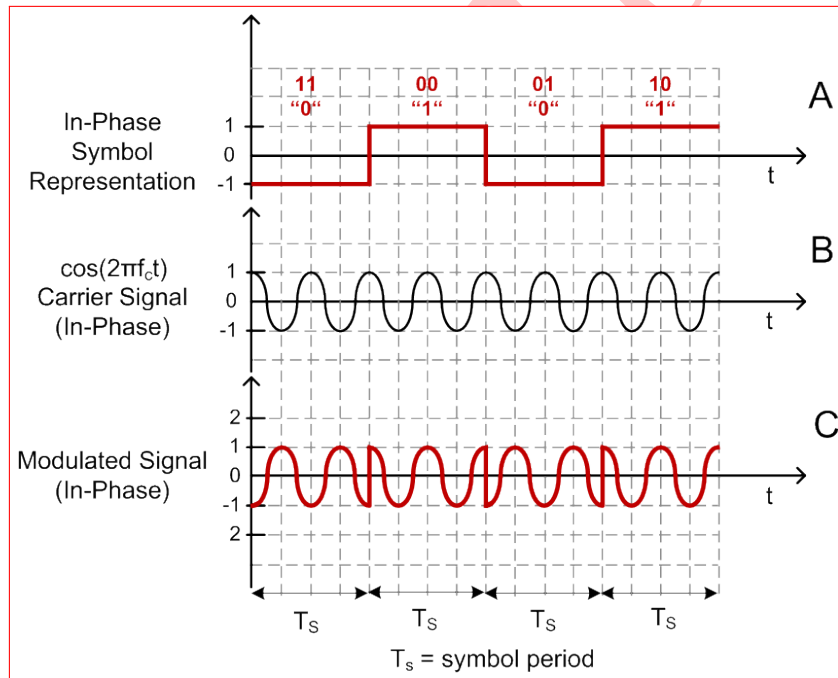
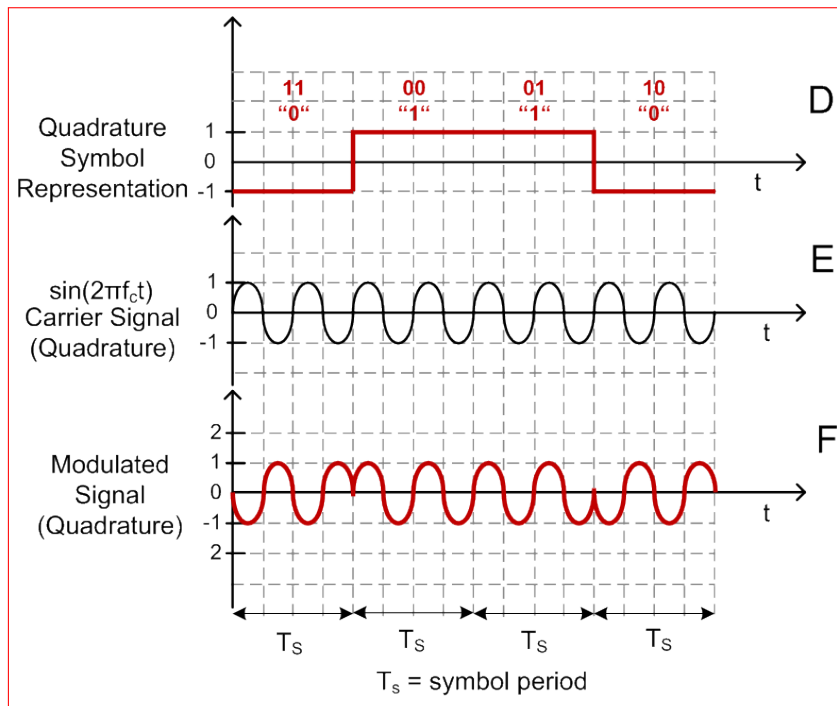


Figure 3.2: A constellation diagram of 4-QAM



1 point for the Sketch A  
1 point for the Sketch C

Figure 3.3: In-Phase symbol representation, carrier signal (in-phase), and modulated signal (in-phase)



1 point for the Sketch D  
1 point for the Sketch F

Figure 3.4: Quadrature symbol representation, carrier signal (quadrature), and modulated signal (quadrature)

### Task 3.2: Spread Spectrum

- A) In Figure 3.5, the power density of a signal is given before and after the spread spectrum technique. The signal A represents the power density before spread and the signal B is after spread. What is the ratio between the area of signal A and the area of signal B?

1

The both areas are the same or equal.

1 point: if the answer is correct

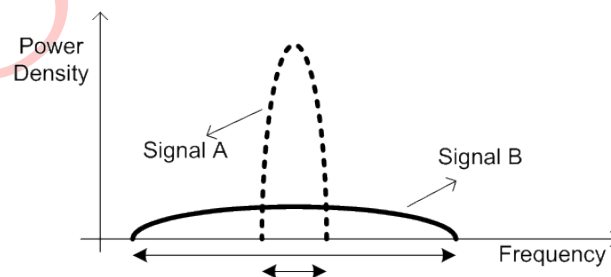


Figure 3.5: A representation of signal's power density vs. signal's frequencies

B) Mention two main requirements for spreading codes used by CDMA.

1

The spectrum of the spread data function shall look like white noise.

0.5 point for each

Spreading functions have to be orthogonal (orthogonal means that the inner product of two functions equals to 0).

requirement

Node	Signal							
0	+1	+1	+1	+1	+1	+1	+1	+1
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	-1	-1	+1	+1	-1	-1	+1
4	+1	+1	+1	+1	-1	-1	-1	-1
5	+1	-1	+1	-1	-1	+1	-1	+1
6	+1	+1	-1	-1	-1	-1	+1	+1
7	+1	-1	-1	+1	-1	+1	+1	-1

Table 3.1: Functions for sender nodes

C) For the simultaneous transmission of four messages, the Walsh functions shown in Table 3.1 shall be used. The nodes 0, 3, 6, and 7 transmit data according to the Table 3.2. Give the resulting signal on the media, make use of the given scheme in Table 3.2.

3

0.5p per correct line,  
0.5p if all lines are  
correct

Node	Data	Signal							
0	"1"	-1	-1	-1	-1	-1	-1	-1	-1
3	"0"	+1	-1	-1	+1	+1	-1	-1	+1
6	"1"	-1	-1	+1	+1	+1	+1	-1	-1
7	"0"	+1	-1	-1	+1	-1	+1	+1	-1
Signal on media		0	-4	-2	+2	0	0	-2	-2

Table 3.2: Transmission with CDMA

- D) The following Signal has been received from a transmission using all the eight Walsh functions from this task.

2

$$+1.1 \ +2.8 \ +2.4 \ +2.0 \ -1.8 \ +4.3 \ -1.0 \ -0.7$$

As corruptions might happen during transmission, the receiver has a tolerance band for the detection. All values differing up to  $\pm 0.5$  from the ideal value will still be accepted. Calculate the bit value that the receiver will detect for node 2, and node 4.

Node 2

Received	+1.1	+2.8	+2.4	+2.0	-1.8	+4.3	-1.0	-0.7
Node 2	+1	+1	-1	-1	+1	+1	-1	-1
	+1.1	+2.8	-2.4	-2.0	-1.8	+4.3	+1.0	+0.7

0.5p for each correct sum  
 0.5p node 2: stating the undefined value  
 0.5p node 4: in detecting "0"

+3.7  $\rightarrow$  undefined value as out of the tolerance band.

Node 4

Received	+1.1	+2.8	+2.4	+2.0	-1.8	+4.3	-1.0	-0.7
Node 4	+1	+1	+1	+1	-1	-1	-1	-1
	+1.1	+2.8	+2.4	+2.0	+1.8	-4.3	+1.0	+0.7

+7.5 is in the tolerance band  $\rightarrow$  a "0" has been detected.

## Task 4: Media Access

### Task 4.1: Multiple Access

Eight different devices communicate on a shared bus-system using TDMA with static time-slot assignment. It can be assumed, that the clocks of each node are perfectly synchronized using a separate clock wire (i.e. clock wire delays are completely compensated). On the data wire, only payload data needs to be transmitted without any additional synchronization overhead. The TDMA cycles (time frames) last for  $t_f = 5ms$  and contain exactly one time-slot for each of the 8 participants. The physical signal propagation delay (one-way delay) between the two most distant nodes on the bus is  $\Delta_{max} = 50\mu s$ . All TDMA time-slots are of equal length and each symbol has a fixed duration of  $t_{sym} = 2.5\mu s$ .

- A) To avoid symbol interference, a guard interval is inserted at the end of each time-slot. How long should this guard interval be at least in order to fully prevent symbol interference in the given system? Calculate the length of the time-slots  $t_{sl}$  as well as the time  $t_{send}$  which can be used for data transmission during a time-slot.

2

The guard time must be at least  $\Delta_{max}$  to avoid symbol interference.

Length of a time slot:  $t_{sl} = t_f/8 = 625\mu s$

The maximum send time then is:  $t_{send} = t_{sl} - \Delta_{max} = 575\mu s$

+1P for guard interval length  
+0.5P for formula  
+0.5 for correct solution

- B) Some of the devices may need to transmit larger amounts of data which can take several seconds. Calculate the average baud-rate  $f_s$  that can be achieved for such transmissions. (If you did not solve the previous question, assume that in each time-slot  $t_{send} = 605\mu s$  can be used for data transmission. )

2

Number of symbols in each time slot:  $n_{sym} = \frac{t_{send}}{t_{sym}} = \frac{575\mu s}{2.5\mu s} = 230$

Frequency of time frames:  $f_f = \frac{1}{t_f} = 200Hz$

Baud rate for one sender:  $f_s = n_{sym} \cdot f_f = 46000Hz = 46kHz$

+1P for correct approach / formula  
+1P for correct solution

**Alternative solution for  $t_{send} = 605\mu s$ :**

Number of symbols in each time slot:  $n_{sym} = \frac{t_{send}}{t_{sym}} = \frac{605\mu s}{2.5\mu s} = 242$

Frequency of time frames:  $f_f = \frac{1}{t_f} = 200Hz$

Baud rate for one sender:  $f_s = n_{sym} \cdot f_f = 48400Hz = 48.4kHz$



## Task 4.2: CSMA/CA

A communication system comprises five communication nodes that use CSMA/CA as arbitration scheme. In order to transmit data a node transmits a dominant start bit (0) for synchronization purpose. After that a 5 bit message identifier followed and 10 bits of payload data is sent. The message identifiers are unique for each node and all data is sent MSB first. The bus has to cover a maximum distance of 500m.

- A) Which requirements have to be fulfilled in order to guaranty a faultless function of the system? What are the implications for the transmission rate?

1

The requirement of simultaneity has to be fulfilled.

The signal propagation time  $t_s$  is much smaller compared to the digit length (bit time)  $t_b$ :

$$\left[ t_s = \frac{l}{v} \right] \ll \left[ t_b = \frac{1}{TR} \right].$$

+0.5P for Simultaneity  
+0.5P for Transmission rate formula or explanation

- B) Table 4.1 shows the identifier of each node. Perform the arbitration phase and fill out the timing diagram in Figure 4.1.

3

Node	identifier
A	10011
B	11001
C	11010
D	10100
E	10100

Table 4.1: Specification of nodes

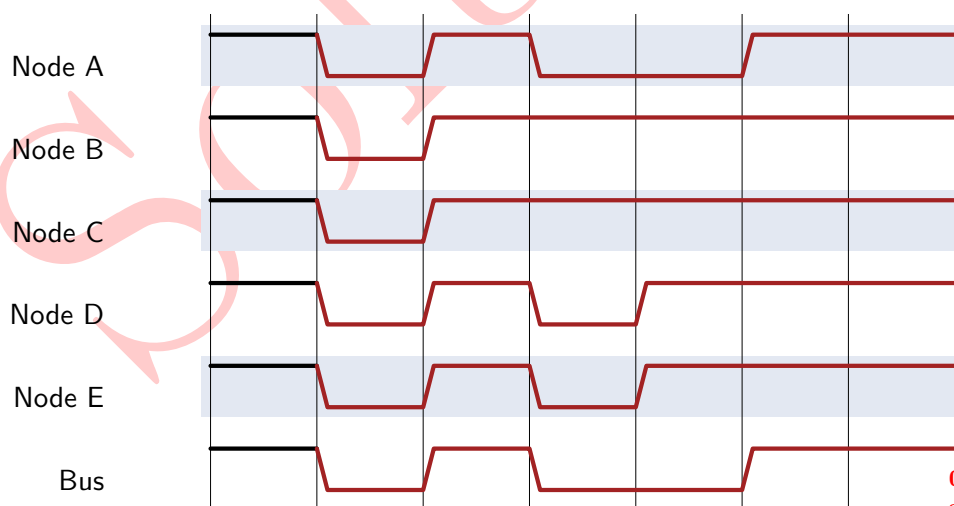


Figure 4.1: Bus Access

0.5P for correct time step (including SOF), no subsequent failure, except SOF missing or dotted line is a failure

- C) Which node is granted exclusive access to the bus?

1

Node A

1P only for correct  
answer**Task 4.3: Arbitration**

A system using polling is shown in Figure 4.2. An exemplary arbitration cycle of the system is shown in Figure 4.3. Signal E is the busy line.

- A) Assign the correct signal lines of Figure 4.2 to the signals shown in the diagram below (Figure 4.3). Justify your choice of signal line assignment with a few sentences. What node is sending data at which point in time? Complete the diagram (Figure 4.3) accordingly and in addition draw the signal line E.

5

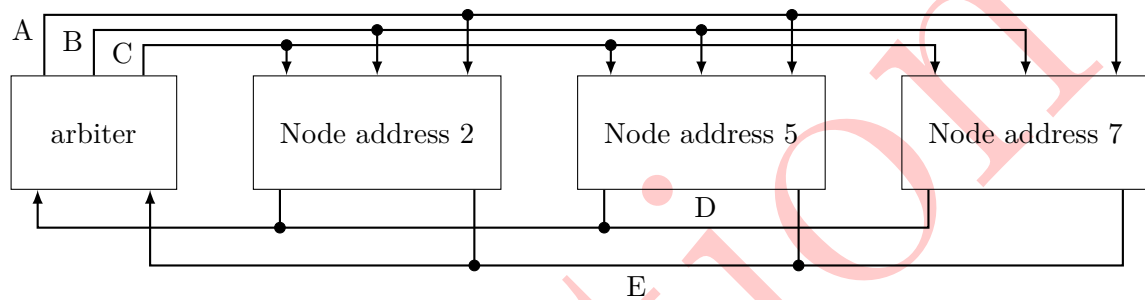


Figure 4.2: Polling

signals D/E - request/busy (high if request/high while data is sent)  
A,B,C - address lines (polling)

1 Point: assign D/ and  
A/B/C  
no points if there is no  
explanation  
1P for each correct  
sender  
1p for signal line E

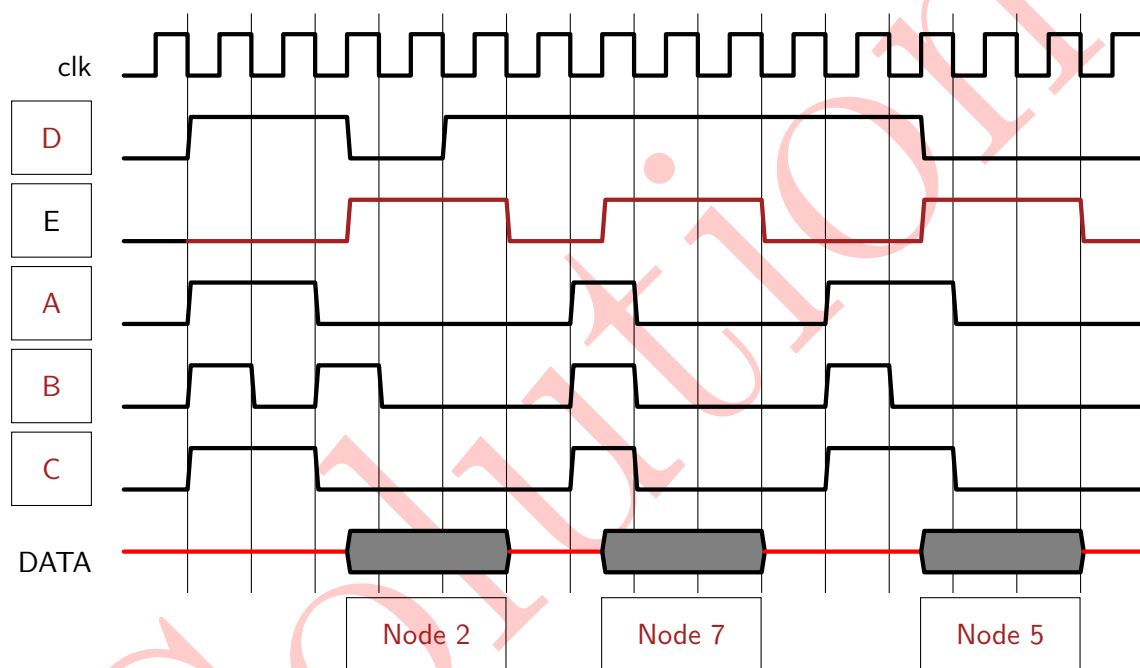


Figure 4.3: Signal flow for Polling

## Task 5: Error Protection

### Task 5.1: Multiple Choice

- A) Specify whether the statements in table 5.1 are true or false.

*Hint: Wrong answers will be penalized. No answer will not give any positive or negative points. The task will be evaluated with a minimum of 0 points.*

3

Statements	True	+0,5P each correct answer -0,5P each wrong answer
The receiver has to use the same CRC generator polynomial as the sender	Yes	
All single-bit errors are detectable with CRC	Yes	
All error bursts > degree of the CRC generator polynomial are detectable		
The error flag (primary) in CAN bus communication is one bit long		
A CAN bus communication node switches into error mode if RX_CNT is higher than TX_CNT		
Security is the protection against malicious errors caused by attackers	Yes	

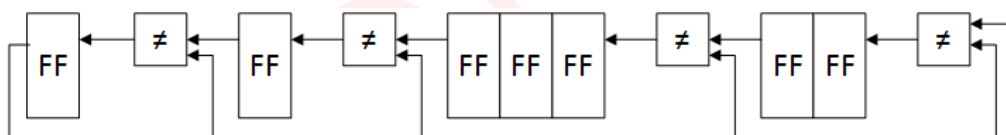
Table 5.1: Multiple Choice

### Task 5.2: CRC-Calculation

- A) To protect data transmission in a mobile device, the given CRC generator polynomial should be implemented. Draw the short form of the linear feedback registers with XOR operators for the given generator polynomial.

Given CRC generator polynomial:  $x^7 + x^6 + x^5 + x^2 + 1$

1



+1P everything is correct

- B) Calculate the data stream that will be transmitted if the following bit stream is to be protected using the CRC generator polynomial given in task 5.2 A):  $x^7 + x^6 + x^5 + x^2 + 1$ .  
Data stream for transmission: **1010 1011**

3

$$\begin{array}{r}
 1010 \ 1011 \ 0000 \ 000 : 1110 \ 0101 \\
 \underline{1110 \ 0101} \\
 0100 \ 1110 \ 0 \\
 \underline{111 \ 0010 \ 1} \\
 011 \ 1100 \ 10 \\
 \underline{11 \ 1001 \ 01} \\
 00 \ 0101 \ 1100 \ 0 \\
 \underline{111 \ 0010 \ 1} \\
 0010 \ 1110 \ 10 \\
 \underline{11 \ 1001 \ 01} \\
 1 \ 0111 \ 110 \\
 \underline{1 \ 1100 \ 101} \\
 0 \ 1011 \ 011
 \end{array}$$

2pt: calculation correct  
0pt if systematic error  
1pt if single calculation error  
0pt if more than 1 calculation error  
1pt for correct complete transmitted bitstream

Bit stream as it is transmitted: 1010 1011 1011 011

- C) In a transmission system that uses CRC for error detection, a receiver receives the following bitstream: **1110 1001 0101**  
Carry out the CRC error detection scheme of the receiver, assuming that the generator polynomial  $x^4 + x^3 + x^2 + 1$  has been used to generate the checksum at the sender. What does the receiver conclude from the result?

2

$$\begin{array}{r}
 1110 \ 1001 \ 0101 : 11101 \\
 \underline{1110 \ 1} \\
 0000 \ 0001 \ 0101 \\
 \underline{1 \ 1101} \\
 0 \ 1000
 \end{array}$$

1,5pt: calculation correct  
0pt if systematic error  
1pt if single calculation error  
0pt if more than 1 calculation error  
0,5pt for the correct statement

The receiver assumes that an error occurred during transmission.

- D) Specify the correct bit stream, assuming that only one bit error has occurred in the transmitted bitstream of the task 5.2 C).

1

correct bitstream: 1110 1001 1101

1pt if correct

### Task 5.3: CAN Bus

A) What are the two main tasks of the ARB Field in a CAN Bus message?

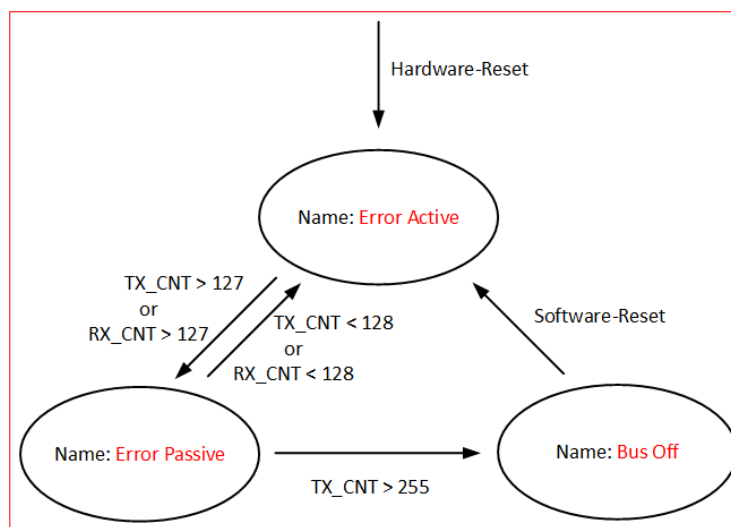
1

- the arbitration which message has the highest priority
- the identification of the message

+0,5p for one correct  
main task

B) In figure 5.1 the error states of the CAN bus communication is shown. Please, fill in the names of the states correctly.

1



-0,5pt for any wrong  
name

Figure 5.1: CAN Error States

C) In a fresh restarted CAN bus communication system only one node acts as sender and transmits a CAN message every 20 ms. Assume that in every 2nd transmission the sender does not receive an ACK (without a following error flag). Assume further that the first successful transmission is done at  $t = 0$  ms. How long does it take until the sender node switches into the Error Passive state?

3

After every error  $\rightarrow TX\_CNT = TX\_CNT + 8$   
 after every successful transmission  $TX\_CNT = TX\_CNT - 1$   
 Condition for transition from Error Active to Error Passive state:  
 $TX\_CNT > 127$   
 $\rightarrow 128 / (8-1) = 18,28... \rightarrow$  after  $18 * 2 + 1 = 37$  transmissions  
 $\rightarrow 37 * 20\text{ ms} = 740\text{ ms}$

+0,5pt for each  
constant ( $Tx+8$ ;  $Tx-1$ ;  
 $Tx>127$ )  
 +1pt for calculation (#  
msg)  
 +0,5pt for correct  
answer in ms

# Task 6: Protocols

## Task 6.1: FireWire Arbitration

The FireWire network shown below is given. The complete self-configuration of the network is already done including initialization, tree identification and self identification.

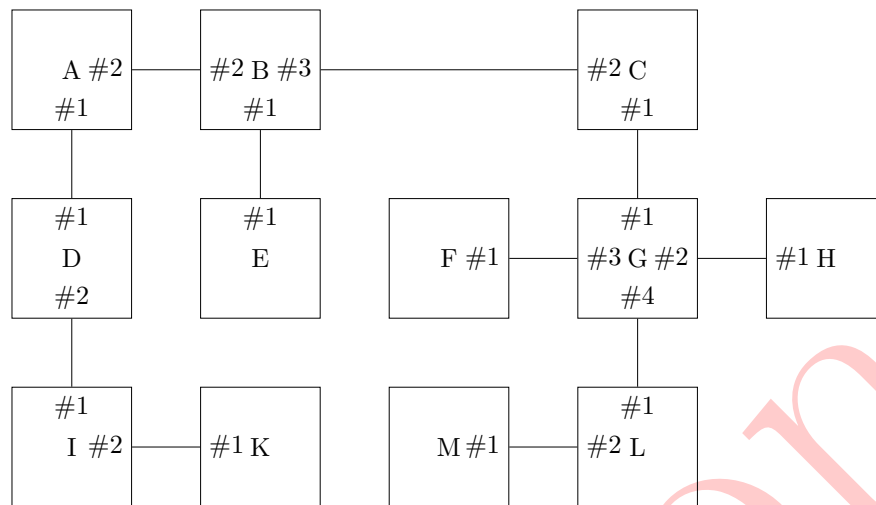


Figure 6.1: FireWire network

Now a normal FireWire bus cycle should be considered. For simplification, several assumptions should be taken into account:

- A list of nodes wanting to send is given.
- All nodes start requesting the bus at the same time.
- Processing of arbitration requests are done in zero time. There are no delays for propagation of the arbitration decision.
- If a node receives multiple bus requests, it will always forward the request that it receives from the port with the lowest number.

A) Mark the root of the FireWire Network in Figure 6.1!

The following nodes request access to the bus: **A, B, C, E, H**. Determine the order in which the nodes will be granted access to the bus.

3

root is node B; access order = B, E, A, C, H

1pt for root  
2pt for correct order  
check order for wrong root

B) If the root sends continuously, it would always grant access to the bus. How does FireWire preserve fairness? Explain your answer for multiple sending nodes **and** only root sending!

2

**multiple nodes sending:** every node is only allowed to acquire the bus once in a cycle. Therefore every node has an arbitration enable bit, that is cleared after a successful access 1pt for multiple nodes  
1pt for root only

**root/one node only:** If there was no access to the bus for a certain amount of time, all nodes reset their arbitration enable bit and a new cycle is started

## Task 6.2: FireWire Structures

- A) Different FireWire structures were built during a student laboratory. During test phase you notice that not all FireWire systems are working. Please state if the FireWire systems given below are working correctly. Mark the roots, if the systems are correct. Give a reason, if the FireWire system is not working correctly.

3

	Correct	Wrong	Reason
	x		
	x		(two individual systems)
	x		Rings are not allowed in FireWire
	x		
	x		Rings are not allowed in FireWire
	x		Rings are not allowed in FireWire

Table 6.1: FireWire structures



### Task 6.3: ITIV-Protocol

The following protocol is used to transfer data between a PC and three wireless weather stations.

The protocol is based on a simple serial data transfer. The transferred data is divided into blocks according to functionalities (Figure 6.2), with the exception of synchronisation (Sync.) with 12 low bits, followed by a high bit. All others follow the rules in Figure 6.3 and Figure 6.4, the exact overview is given below.

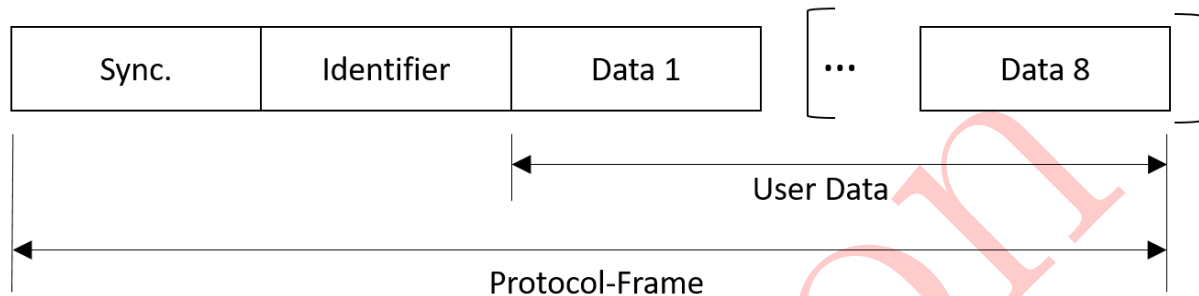


Figure 6.2: Structure of a protocol frame

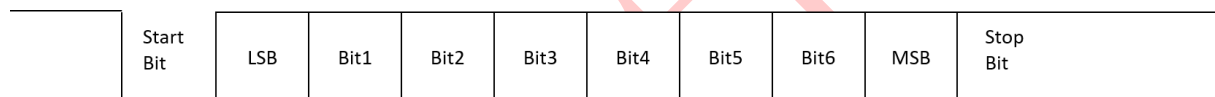


Figure 6.3: Bit sequence within a block

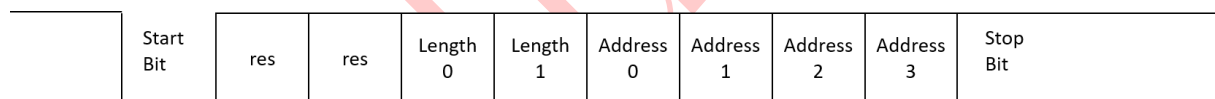


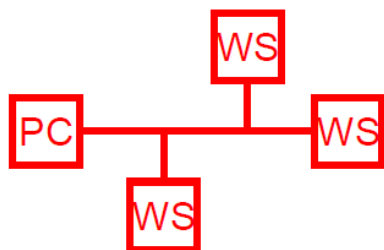
Figure 6.4: Structure of the identifier field

- A) Draw the structure of the wireless network! What kind of topology (analogous to wired structures) is the network?

2

It is a bus topology, as all participants share one medium.

1pt drawing,  
1pt name of topology



- B) Use the protocol to determine the maximum number of slaves that can be addressed within a network. Justify your answer!

**1**

$2^4 = 16$  Slaves

- C) How many bits does a transmission from the master to the slave with the address 0x02 take, if 4 user bytes are sent?

**1**

Protocol + 4 Bytes = Sync + ID + 4 Bytes = 13 + 10 + 4\*10 = 63

**0 if wrong**

- D) A datastream consisting of the same bits as the "sync." should be transmitted. Do you need to modify the protocol in order to transmit this data? If Yes: Explain how! If no: Why not?

**2**

No modification or bitstuffing is necessary, because of start/stop after 8 bits

**1Pt for no modification  
1Pt for start/stop bits**

# Task 7: Routing

## Task 7.1: Router and Switching

- A) Explain the functionality of a router and its components as defined in the lecture, the components are routing control, message buffer and switch matrix.

2

router switches paths and decides on the direction of the data

each half Point

routing control determines what input is connected to what output

message buffers incoming data, multiple packets

switch matrix electrically connects inputs to outputs

- B) The switch matrix of a router can be implemented using full crossbars or reduced crossbars. Describe the differences between both in terms of hardware resources and routing capabilities.

2

full crossbars imposes no limitations on routing while reduced crossbars limit concurrent connections

each one Point

Hardware consumption is smaller for reduced crossbar

- C) Describe a reasonable way to implement the routing control and message buffers of a router.

1

routing control can be implemented as a Look Up Table

each half Point

message buffers can be implemented as FIFO memory

There are multiple answers, buffers should be some kind of memory and control logic

- D) Describe the implications of circuit and packet switching to the routing control and message buffers of a router ? How are they different and why ?

2

message buffers have to be used for packet switching

message buffer answer  
1p routing ctrl 1p

message buffers are not necessary for circuit switching

routing control needs to have support of setup phase for circuit switching

routing control needs pathfinding for every packet when using packet switching

## Task 7.2: Routing

A) Name and describe 2 categories that can be used to classify routing algorithms !

2

Static (Deterministic) and Dynamic (Adaptive) ; predefined paths or calculated on the fly

Distributed and Source routing route is calculated by sender or nodes in network

Minimal Routing and Non-Minimal Routing shortest vs not shortest path

There are 6 categories here. +1 point for naming any two category and giving its description.

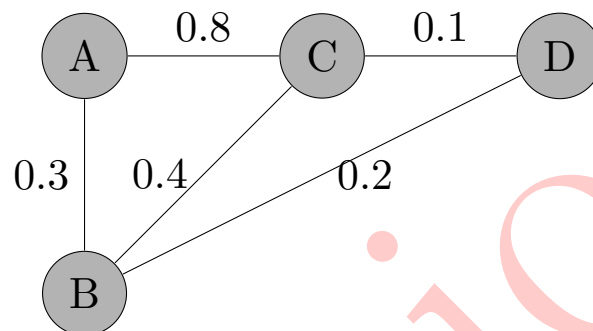


Figure 7.1: Given network topology

B) Figure 7.1 represents a network for which an optimal routing has to be found. The weights represent the error rate of each connection. With node A as the starting point, calculate the paths with the lowest error rates in the network by using Dijkstra's algorithm. For that write down the order in which nodes are visited in each bracket under the current step and fill out the given tables that encompass the shortest paths after each visitation of a node.

3

	step 1		step 2		step 3		step 4		step 5	
node	A		A		B		D		C	
vertex	err.	pred.	err.	pred.	err.	pred.	err.	pred.	err.	pred.
A	$\infty$	A	0	A	0	A	0	A	0	A
B	$\infty$	-	0.3	A	0.3	A	0.3	A	0.3	A
C	$\infty$	-	0.8	A	0.7	B	0.6	D	0.6	D
D	$\infty$	-	$\infty$	-	0.5	B	0.5	B	0.5	B

Table 7.1: Dijkstra's algorithm

step 2,3,4 0.5 point  
step 5 1 point  
correct nodes in the  
node row 0.5 point

- C) Describe a scenario in which the connection between the nodes A and C from Figure 7.1 would be preferable, compared to a connection with lower error rate !

1

If performance is the key objective, the combination of latency/throughput and error rate would yield the metric to be considered. A connection with lower error rate might be so slow that it would be worse.

one point for a  
reasonable scenario

Again several answers, they just have to be reasonable

- D) Describe a scenario and explain why the Dijkstra algorithm is more suitable for routing than XY-Routing !

1

Non mesh based topologies

weights represent something different than (manhattan) distance

0.5 point for each or  
providing a reasonable  
scenario and  
explanation

## Task 8: Network Topologies

### Task 8.1: General Questions

- A) There are four topologies given: 4x2x2 Mesh, 4x4 Torus, Star, Ring. Assume that each topology contains 16 nodes. Give the value of edge connectivity, diameter and resource cost (i.e. in this case the total number of bi-directional links). Use the following table to provide your answers.

6

Network	Edge Connectivity	Diameter	Resource Cost
4x2x2 Mesh	3	5	28
4x4 Torus	4	4	32
Star	1	2	15
Ring	2	8	16

for each correct answer: +0,5

Table 8.1: Metrics and topologies

### Task 8.2: 4D Topology

When we increase the amount of nodes in a mesh, it can be useful to scale the mesh into a higher dimension instead of adding the nodes in the same dimension. A higher dimension keeps the diameter low while increasing the edge connectivity of the nodes.

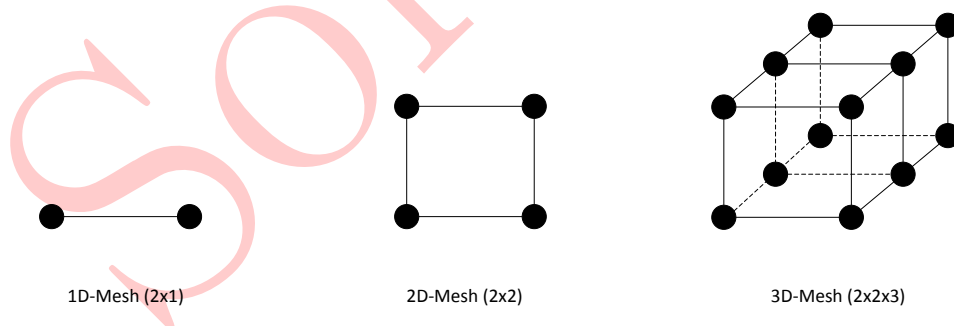


Figure 8.1: Drawing higher-dimensional meshed networks

For drawing higher dimensional mesh topologies on a sheet of paper, some techniques exist. If we consider a 1-dimensional topology consisting of two nodes and want to move towards a 2-dimensional (2x2) topology, we simply copy our original nodes and connect each node with their exact copy. For a 2x2x3 topology, we copy the existing 2x2-rectangle two times (resulting in 3 rectangles) and connect each original node with their first copy and their first copy with the second copy. The same technique can be applied to a 4D topology, where we copy our 3D cubes and connect each node to its next copy.

4

A) Assume a  $4 \times 2 \times 5 \times 3$  mesh topology for this task. Each node can be described by the tuple  $(x_1, x_2, x_3, x_4)$ . Find the shortest path from the source point  $(4, 0, 2, 3)$  to the destination point  $(1, 1, 3, 1)$ . Thereby, the routing policy that each node has to obey is described as follows:

1. Try first to route in the direction of the largest vector component from the current router's position towards the destination. The vector components are  $\|\Delta x_1\|$ ,  $\|\Delta x_2\|$ ,  $\|\Delta x_3\|$ ,  $\|\Delta x_4\|$ .
2. In case there are multiple directions with the same largest value for the respective vector components possible, prioritize first  $x_1$  then  $x_2$  then  $x_3$  and finally  $x_4$  among the directions with the largest vector components.

In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence.

$(4, 0, 2, 3) \rightarrow (3, 0, 2, 3) \rightarrow (2, 0, 2, 3) \rightarrow (2, 0, 2, 2) \rightarrow (1, 0, 2, 2) \rightarrow (1, 1, 2, 2) \rightarrow (1, 1, 3, 2) \rightarrow (1, 1, 3, 1)$

+0.5 pts per intermediate step (start and end point are optional and don't give extra points)  
+1 pt for a full solution with no errors -0.5 pt for wrong step

4

B) A fault is now present in the router at node  $(1, 1, 2, 1)$ . Due to this fault the router behaves as described below.

1. The router tries to route in the direction of the largest vector component from the current router's position **away from** the destination. The vector components are  $\|\Delta x_1\|$ ,  $\|\Delta x_2\|$ ,  $\|\Delta x_3\|$ ,  $\|\Delta x_4\|$ .
2. In case there are multiple directions with the same largest value for the respective vector components possible, prioritize first  $x_1$  then  $x_2$  then  $x_3$  and finally  $x_4$  among the directions with the largest vector components.

The other routers in the network are not aware of the fault in this router and will perform the routing without changing their strategies. Now route a packet starting from  $(4, 1, 2, 1)$  towards  $(1, 1, 3, 1)$  and name all visited nodes. Does the packet still reach its destination even with the faulty router? Explain your answer.

$(3, 1, 2, 1) \rightarrow (2, 1, 2, 1) \rightarrow (1, 1, 2, 1) \rightarrow (1, 1, 1, 1) \rightarrow (1, 1, 2, 1)$ . No, the packet does not reach the destination. Because there is a loop in the path/ Because livelock is present.

+0.5 pts for mentioning each visited node (start and end points do not give points). -0.5 pt for wrong step  
+1.5 pt for mentioning that the packet does not reach the destination and giving a reasonable explanation.

C) Explain the difference between a livelock and a deadlock in a network.

1

In a livelock, the system still continues but a transmission never reaches its destination (due to e.g. circles) while in a deadlock, the system is stuck due to mutual blocking of links. +1 pt for Explanation

D) What is the edge connectivity and the diameter of a 4x2x5x3 mesh topology?

1

edge connectivity = 4

+0,5 for each answer

diameter = 10